CprE 281 HW12
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Analysis of Synchronous Sequential Circuits, ASM charts/examples
Finish by Nov. 27, 2023

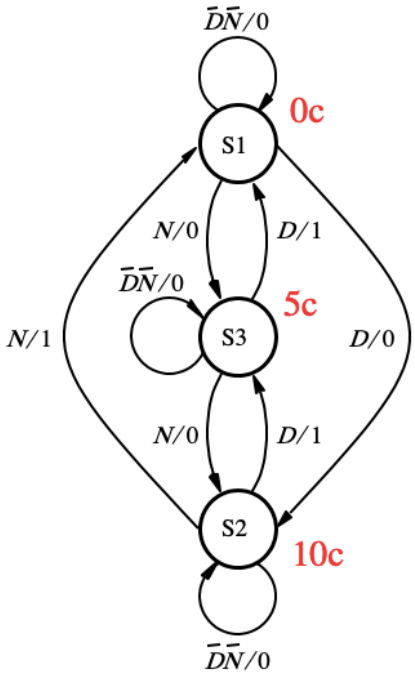
P1. (15 points): Draw the circuit diagram for the following FSM state table.

a) What type of machine is this? Moore or Mealy? Why?
b) Derive the state-assigned table.
c) Derive the truth tables for Y_1, Y_0, and z.
d) Draw the K-maps and derive the expressions.
e) Draw the circuit and add the reset line

Present state	Nextstate		Output z
	w = 0	w = 1	
A	B	C	1
B	A	F	1
C	F	C	0
F	C	A	0

P2. (15 points): Draw the circuit diagram for the vending machine FSM graph.

a) Derive the state table for this Mealy machine.
b) Derive the state-assigned table.
c) Derive the truth tables for Y_1, Y_0, and z.
d) Draw the K-maps and derive the expressions.
e) Draw the circuit and add the reset line



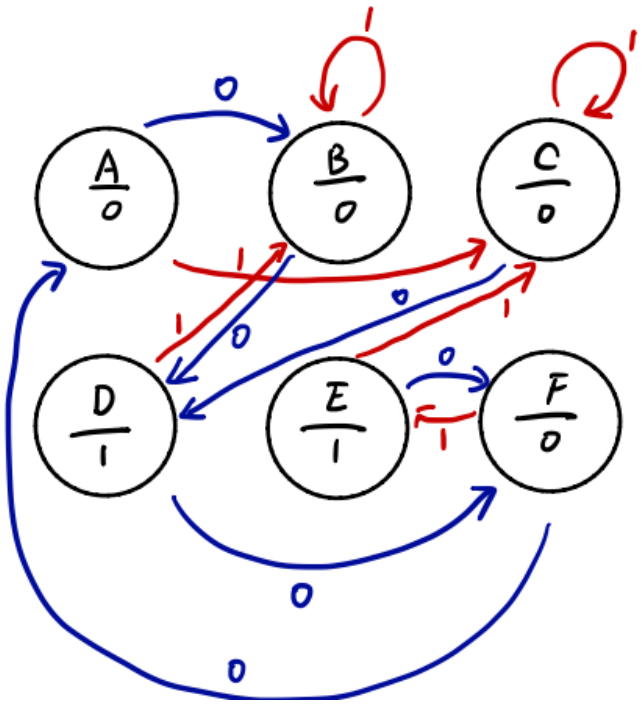
P3. (15 points) Two-bit up-counter.
Use the synchronous sequential circuit approach to design a two-bit up-counter. The circuit should have one input w. If w=1 the count is incremented. If w=0 the current count remains the same. The counter sequence should be: 0, 1, 2, 3, 0, 1, …

a) Draw the state diagram.
b) Draw the state table.
c) Draw the state assigned table.
d) Write down the logic expressions for the next state variables and the output.
e) Draw the circuit diagram [use the next page if you need space.

P4. (15 points) Consider a 3-bit up-counter that only counts prime numbers, starting from 2, and then repeats the sequence. Draw this counter with minimal number of states.

a) Draw the state diagram for the counter.
b) Construct the state-assigned table, including the next state and output.
c) Draw the circuit diagram.

P5: (10 points): Perform state minimization for the following FSM state diagram/graph. If it is not possible to reduce the number of states, say that minimization is not possible.



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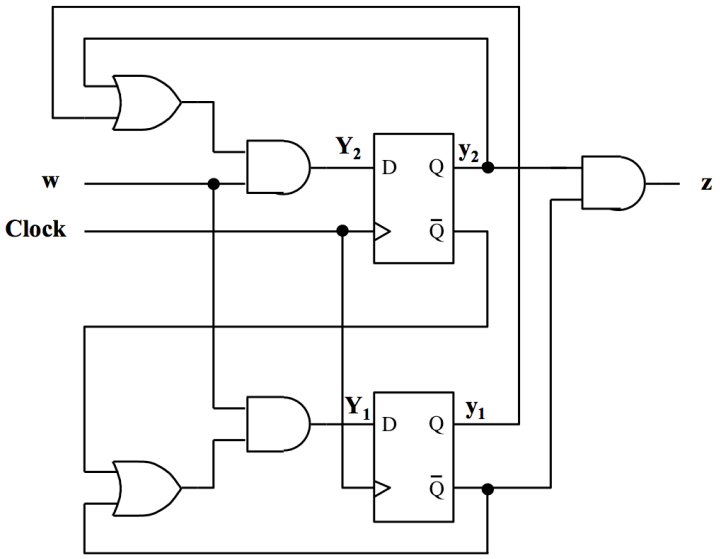
P6. (15 points) Reverse engineer the following circuit. That is, derive the following:

a) Logic expressions.
b) State-assigned table.
c) State table.
d) State diagram/graph.
e) Also, explain with words the functionality of this FSM (i.e., what sequence of input values on w is detected by this circuit when it sets z to 1? What happens when it reads a zero or a couple of zeros from the input?)



P7. (15 points) Reverse engineer the following circuit. Follow the steps from P6.