Name and Std ID:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Lab Section:\_\_\_\_\_\_

Date:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**PRELAB:**

**Q1.** Read section 2.2 and write the Verilog code for a 4-to-1 multiplexer.

**Q2.** Design a 4-bit shifter as described in Section 3.1 of the lab description. Sketch the block diagram for your design showing the multiplexers, the inputs, outputs and the selectors to each multiplexer.

**Q3.** Refer to Section 3.1 of the lab description and complete the following table before you come to the lab:

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **X3** | **X2** | **X1** | **X0** | **Xc1** | **Xc2** | **Xc3** | **S1** | **S0** | **F3** | **F2** | **F1** | **F0** |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |  |  |  |  |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |  |  |  |  |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |  |  |  |  |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |  |  |  |  |

TA Initials: \_\_\_\_\_\_\_\_\_

**LAB:**

**2.4**  Hardware results demonstrate a good circuit. TA Initials: \_\_\_\_\_\_\_\_\_

**3.1**  ModelSim results demonstrate correct code. TA Initials: \_\_\_\_\_\_\_\_\_