

PRELAB!

Read the entire lab, and **complete** the prelab questions (Q1-Q3) on the answer sheet **before** coming to the laboratory.

1.0 Objectives

In Lab 4, you designed a multiplexer. In this lab, you will learn to design shifters using multiplexers. You will design a 1-bit 4-to-1 Multiplexer in Verilog; afterwards, you will use this newly-designed multiplexer to build a shifter circuit.

2.0 Multiplexers

2.1 A 4 to 1 Multiplexer (1-bit)

The following is the Verilog code for a 1-bit 2 to 1 multiplexer. When the selector s is 0 the output f is $i0$ and when the selector s is 1 the output is $i1$.

```
module mux2to1(i0, i1, s, f);  
    input i0, i1, s;  
    output f;  
    assign f = s ? i1 : i0; //The ternary operator looks at  
    //the bit value before the ? (which is s) and will either  
    //assign the value to the left of the : (which is i1) to f if s is 1  
    //or assign the value to the right of the : (which is i0) to f if s is 0.  
endmodule
```

Modify this code to build a 1-bit 4-to-1 multiplexer. The multiplexer will have the following specification:

- Four 1-bit data inputs, $W0$, $W1$, $W2$ and $W3$.
- One 2-bit selector input, S [1:0].
- One 1-bit output, F .
- When $S[1:0] = 00$ the output will be $W0$.
- When $S[1:0] = 01$ the output will be $W1$.
- When $S[1:0] = 10$ the output will be $W2$.
- When $S[1:0] = 11$ the output will be $W3$.

For a detailed explanation of multiplexers, please refer to the textbook. Also, read and understand any code that you may find in your textbook for multiplexers. *Note: It will be easier to reuse this code if you do not use a bus for the W inputs.*

2.2 Bus Notation in Schematic Files

To create a bus in a schematic file (i.e. block design files), you will use the following syntax:



Fig 1. A Schematic Bus

The example above creates a bus input named S that is two bits wide. Notice that there are **two (2)** periods between the numbers in the brackets. This indicates that there is a wire on bus line 1 and a wire on bus line 0. This also indicates that bus line 1 represents the most significant bit of these two bus lines.

To connect to individual lines on a bus, you have to use the orthogonal node tool and give the node a name that references the **name** of the bus followed by the **bit position** of the bus you want to connect. You can also connect to a subset of lines of a bus using the orthogonal bus tool using the same naming paradigm as above.

2.3 Bus Notation in Verilog Files

To create a bus in Verilog, use the Verilog bus syntax as demonstrated in the example below:

```
module mux2to1_4bit(A, B, S, F);  
  input [3:0] A;  
  input [3:0] B;  
  input S;  
  output [3:0] F;  
  // Buses in Verilog use : instead of ..  
  
  assign F = S ? B : A;  
endmodule
```

The Verilog syntax uses a **colon** to indicate a bus **instead** of two periods. Note that each bus should be defined on its own line, which is separate from other buses of different widths and single bit inputs/outputs. To access a certain bus line, use the following syntax:

For the previous example:
F[3] represents the most-significant bit of the mux output.
F[0] represents the least-significant bit of the output.

Here, F is the bus name and the bus line index is placed in square brackets.

2.4 Testing Your 4-to-1 Multiplexer

Create a new folder and a new project (*mux4to1*). Save the Verilog code for the 1-bit 4-to-1 multiplexer as *mux4to1.v*. Use the DE2-115 board to test your code. Assign pins for the daughter board as follows:

- Connect the four pins for W0, W1, W2, and W3 to the four rocker switches.
- Connect the two pins for S to the two push-buttons.
- Connect the output F to any LED.

Note that the push-buttons on the daughter board output a logic 1 only when they are pressed down. The push-buttons on the parent board, however, behave differently and output a logic 0 when they are pressed down.

When you are confident that your code is correct, show your results to your TA. Once you are done create a default symbol for your mux4to1 so that you can use it in the next section.

3.0 Shifters

3.1 Designing a Shifter

You will now design a device called a shifter. A Shifter is built from multiplexers and shifts the outputs, based on the select signals. For this shifter, you will use 1-bit 4-to-1 multiplexer of Section 2.2. A shifter has the following inputs and outputs:

X3, X2, X1, X0

Xc1, Xc2, Xc3

S1, S0

F3, F2, F1, F0

Primary Inputs

Cascading Inputs

Shift Count

Fixed Outputs

The shifter outputs the inputs shifted to the left 0, 1, 2, or 3 places as indicated by the 2-bit shift count (select signals). The table below summarizes the behavior:

S1	S0	F3	F2	F1	F0
0	0	X3	X2	X1	X0
0	1	X2	X1	X0	Xc1
1	0	X1	X0	Xc1	Xc2
1	1	X0	Xc1	Xc2	Xc3

Example:

Let the inputs have the values below:

X3	X2	X1	X0	Xc1	Xc2	Xc3
0	1	1	0	1	0	1

If the shift count is 00, the output would be:

F3	F2	F1	F0	Xc1	Xc2	Xc3
0	1	1	0	1	0	1

If we shifted left ONE position – i.e., shift count is 01 then the output would be:

X3	F3	F2	F1	F0	Xc2	Xc3
0	1	1	0	1	0	1

The result makes it look like the **Shift Count** moves the window for the output!

To develop this Shifter, start with a new block diagram. Name it as your top-entity-file. The default should be *lab8step2.bdf*.

To complete the shifter design you will need four 1-bit 4-to-1 multiplexers, one for each output of the shifter. As is evident from the table summarizing the behavior of a shifter, the output bit F3 of the shifter can be X3, X2, X1 or X0 depending on the value of the shift count. A 4-to-1 multiplexer allows choosing from X3, X2, X1 and X0 based on the value of the shift count.

For this circuit, you will only place **one output pin** on the block diagram and name it **F[3..0]**. Next, create a small node line (orthogonal node tool) on the output of each mux. Then, run a bus line (orthogonal bus tool) to the output pin and connect each node line to the bus line. You should now have the output of each mux connected to the same bus line via a node line. Next, you must label each node line to establish its position in the bus. To do this, simply right click the node line and give it a name. An example is shown below in **Figure 1**.

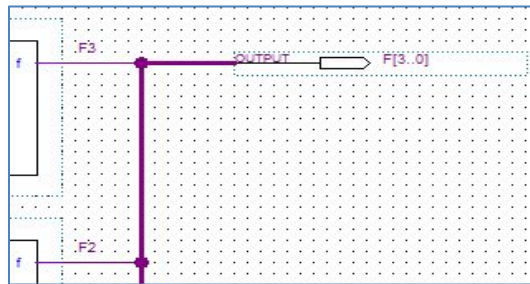
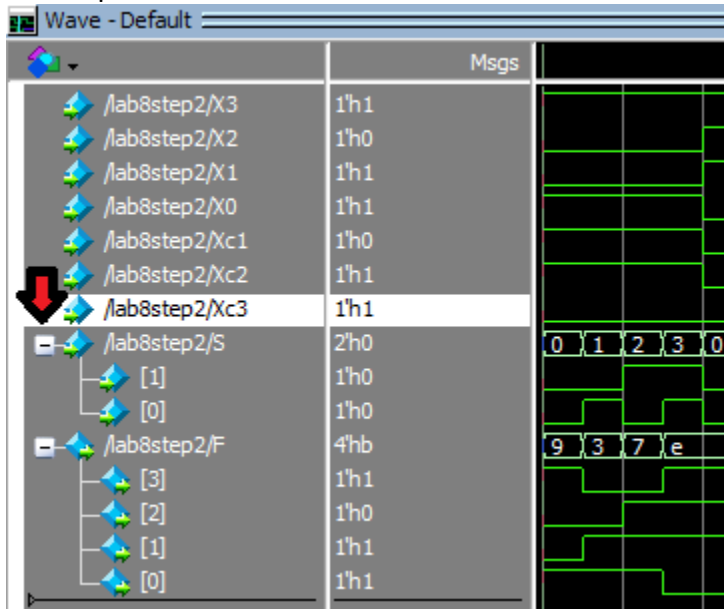


Figure 1: Node Line to Bus Line Connections

Once your circuit is ready: create a Verilog HDL and simulate your shifter on ModelSim. Use a DO file to simulate the Primary and Cascading inputs based on the table you filled out for prelab Q3, but allow the 2-bit input S to cycle through all values. You may use **shifter.do** to simulate your results.

Note: As your shifter has 2-bit input bus S and 4-bit output bus F, you will have to click on the plus in order to see the waveforms for the individual bits on the bus.



Once you understand your circuit, follow the table you filled out for prelab **Q3** and demonstrate the proper operation of your shifter to the TA.

4.0 Complete

You are done with this lab. Close all lab files, exit Quartus Prime, log off the computer, power down the DE2-115 board, and hand in your answer sheet. **Don't forget to write down your name and your lab section number.**