Name and Std No.:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Lab Section:\_\_\_\_

Date:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**PRELAB:**

### *Refer to Chapter 5 in your textbook and the lab instructions to complete your pre-lab. Please read all the material and complete the circuit diagrams before you come to the lab.*

**Q1.** Draw the circuit diagram for the SR Latch using NOR Gates for **Section 2.0** in the space below.

**Q2.** Draw the circuit diagram for the $\overbar{S}\overbar{R}$ Latch using NAND Gates for **Section 2.0** in the space below.

**Q3.** Draw the circuit diagram for the D Latch using NAND Gates and a NOT gate for **Section 3.0** in the space below.

**Q4.** Draw the circuit diagram for the D Flip-Flop for **Section 4.0** using the D latches you built in the previous step in the space below. The flip-flop should be triggered by the negative edge of the clock.

**Q5.** Draw the circuit diagram for the Positive-Edge-Triggered D Flip-Flop using NAND gates for **Section 4.0** in the space below.

Prelab TA Initials: \_\_\_\_\_\_\_\_

**LAB:**

 **2.0** Complete the characteristic table for both versions of the SR latch. Do both versions function properly as a latch? \_\_\_\_\_\_\_\_

|  |  |  |
| --- | --- | --- |
| **SR NOR Latch** |  | $\overbar{S}\overbar{R}$ **NAND Latch** |
| **S R** | **Action** |  | **S R** | **Action** |
| 0 0 | *Keep State* |  | 0 0 |  |
| 0 1 | *Q =*  |  | 0 1 | *Q =*  |
| 1 0 | *Q =*  |  | 1 0 | *Q =*  |
| 1 1 | *Restricted Combination* |  | 1 1 |  |

ModelSim results demonstrate a good circuit. TA Initials: **NOR**\_\_\_\_­\_\_\_ **NAND**\_\_\_\_\_\_\_

**3.0** Complete the timing diagram below for your Gated D Latch.

What is the difference between this gated latch and the previous basic latches?

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Clk** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **D** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **Q** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Hardware results demonstrate a good circuit. TA Initials: \_\_\_\_­\_\_\_

**4.0** Complete the timing diagram below for your Negative-Edge-Triggered D Flip-Flop.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| **Clk** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **D** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **Q** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **~Q** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Hardware results demonstrate a good circuit. TA Initials: \_\_\_\_­\_\_\_

Complete the timing diagram below for your Positive-Edge-Triggered D Flip-Flop.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Clk** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **D** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **Q** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **~Q** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Hardware results demonstrate a good circuit. TA Initials: \_\_\_\_­\_\_\_