Cpr E 281 LAB12
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Lab 12 Answer Sheet

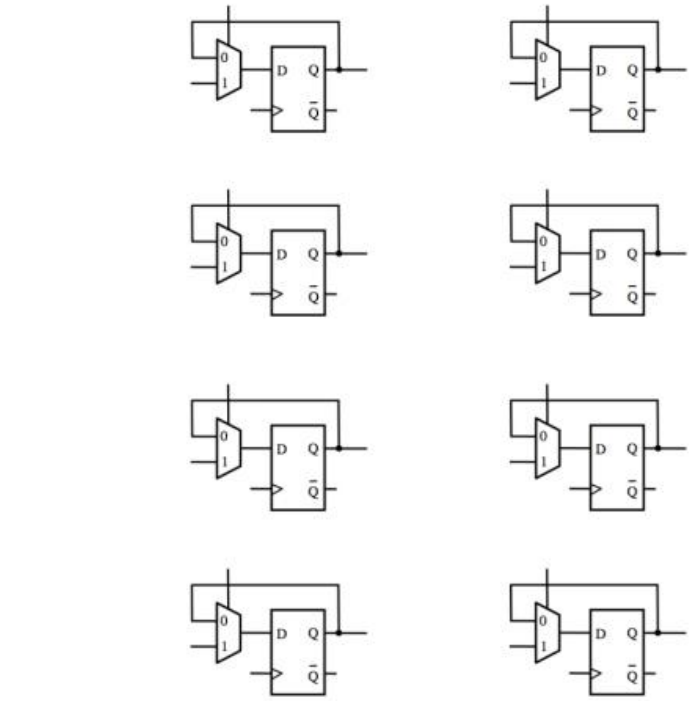
Name and Student ID:_____ **Lab Section:**__

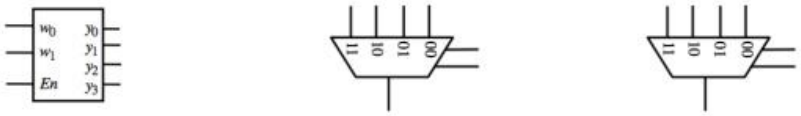
Date:_____

PRELAB:

Q1. Circuit diagram for a register file with four 2-bit registers.

Please complete the following circuit diagram to implement a register file with four 2-bit registers, one write port, one read port, and one write enable line. Label all inputs and outputs of your circuit. Please use different colors for the different types of wires.





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The rest of this lab is about a register file with <u>eight</u> 4-bit registers.

Q2. Draw a schematic diagram for a 4-bit register using four D Flip-Flops and four 2-1 multiplexers. Draw a block around each one-bit register used in your design.

Q3. Write the Verilog code for a 4-bit 8-to-1 multiplexer below.

```
module Mux8_4b(S2, S1, S0, W0, W1, W2, W3, W4, W5, W6, W7, F);
   input S2, S1, S0;
   input [3:0] W0, W1, W2, W3, W4, W5, W6, W7;
   output [3:0] F;
```

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Q4. Write the Verilog code for a 3-to-8 decoder in the space below.

```
module Decoder3to8(EN, W2, W1, W0, Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7);
   input EN, W2, W1, W0;
   output Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7;
```

Q5. Using copies of the decoder, multiplexer, and 4-bit register from the previous steps, write the Verilog code that will provide the functionality of a register file with eight 4-bit registers. Your code should contain the decoder, the 4-bit registers, the multiplexers, and additional connections to make the whole circuit operational.

```
module regfile(DATAP3, DATAP2, DATAP1, DATAP0, DATAQ3, DATAQ2, DATAQ1, DATAQ0,
   RP2, RP1, RP0, RQ2, RQ1, RQ0, WA2, WA1, WA0, LD_DATA, WR, CLRN, CLK);

   // address and control ports
   input RP2, RP1, RP0, RQ2, RQ1, RQ0, WA2, WA1, WA0, WR, CLRN, CLK;

   // input data port
   input [3:0] LD_DATA;

   // output data ports
   output DATAP3, DATAP2, DATAP1, DATAP0, DATAQ3, DATAQ2, DATAQ1, DATAQ0;

   // wire declarations
   wire [3:0] DATAP, DATAQ;
```

Prelab TA Initials: _____

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LAB:

Fill in the characteristic table for the one-bit parallel access register.

In	Load	Out
0	0	
1	0	
0	1	
1	1	

Fill in the table with steps that will load the registers as follows: Reg[0]=F, Reg[1]=A. Reg{2]=C. Reg[3]=E, Reg[4]=2, Reg[5]=7, Reg[6]=6, and Reg[7]=1.

LD_DATA	WA

4.0 Register File with Eight 4-bit Registers

Hardware demonstrates a good circuit. TA Initials: _____

Fill in the table below with the result produced by the register file (with CLRN=1).

LD_DATA	Sel	WA	RP	RQ	CTRL	WR	Effect
0110	0	111	111	111	0	1	Reg[7] ← 6.
0011	0	110	110	111	0	1	
0010	0	101	101	110	1	1	
0100	0	100	100	101	1	1	
0101	0	011	011	100	0	1	
0001	0	010	010	011	0	1	
0111	0	001	001	010	1	1	
1000	0	000	000	001	1	1	Register File Contents:
0000	1	001	000	001	0	1	
0001	1	000	010	011	0	1	
1111	1	010	100	101	1	1	
1001	1	101	110	111	1	1	
0100	1	010	010	101	1	0	Register File Contents:

5.0 Register File with Adder and 7-Seg Displays

Hardware demonstrates a good circuit. TA Initials: _____