CprE 2810 HW7

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Multiplexers and Decoders

Assigned Date: Eighth Week
Finish by Oct. 21, 2024

P1 (10 points). Design and construct a hierarchical multiplexer system.

a. Design a 16-to-1 multiplexer using a minimal number of 2-to-1 multiplexers. Draw the block diagram and clearly label all signals, including control lines.

b. Design a 16-to-1 multiplexer using a minimal number of 4-to-1 multiplexers. Draw the block diagram and clearly label all signals, including control lines.

P2 (15 points). Consider the Boolean following Boolean function:

$$F(A, B, C) = A'B\ C' + ABC$$

a. Draw the truth table for this function.
b. Use the hierarchical divide-and-conquer method to partition the truth table. Write the value of the function for each of the smallest partitions. This will help you design the circuit in part c. Hint: the first partition is by A; the second partition is by B, but it is performed twice.
c. Draw a logic circuit that implements this function using **only** 2-to-1 multiplexers. No other logic gates are allowed. If you need to negate a signal you must use a multiplexer for that as well. Clearly label all signals and show the connections between the multiplexers.

P3 (10 points). Implement a 2-to-4 decoder with enable using only 1-to-2 decoders with enable. How many do you need? Draw a circuit diagram.

P4 (15 points). Consider the Boolean function:

$$F(w_1, w_2, w_3) = \overline{w_1}\ \overline{w_2} + \overline{w_2}\overline{w_3} + w_1 w_2 w_3$$

a. Derive a new expression that uses Shannon's theorem, with respect to w_1.
b. Derive a new expression that uses Shannon's theorem, with respect to w_2.
c. Derive a new expression that uses Shannon's theorem, with respect to w_3.

P5 (10 points). Answer the following questions about decoders and multiplexers. For all subparts, please explain your reasoning. Assume that all decoders are decoders with enable. No need to draw circuit diagrams for this problem.

a. How many 2-to-4 decoders and 4-to-16 decoders would you need if you must construct a 6-to-64 decoder? Explain.

b. How would you implement a 64-to-1 multiplexer using a combination of 8-to-1 and 2-to-1 multiplexers? Explain.

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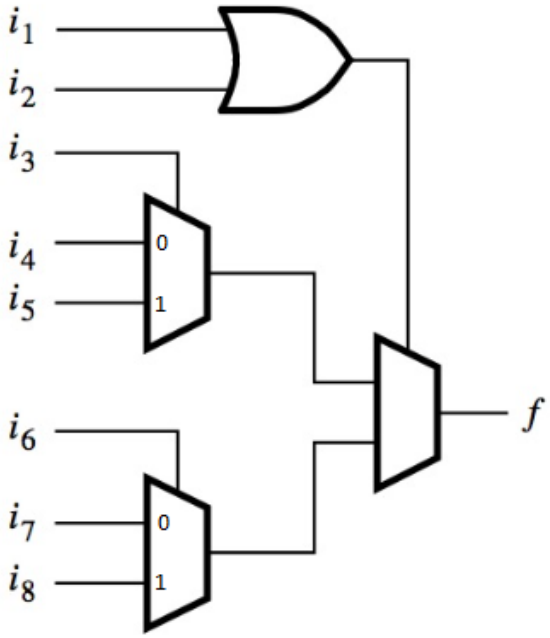
P6 (15 points). Consider the multiplexer-based circuit illustrated below. Show how this Boolean function

$$f(w_1, w_2, w_3) = w_1 w_2 \overline{w_3} + w_1 w_3 + w_2 w_3$$

can be implemented using only one instance of the provided circuit. Clearly explain how each input and selector in the circuit is used to implement the given function. Clearly state which signal is provided to which of the 'i' signals. Assume that all signals are given to you in non-inverted form. The constants 0 and 1 are also provided.



P7 (10 points). Implement this function using **only** 2-to-1 multiplexers and no other logic gates

$$f = a'b\,c + a\,b'c' + ab'c$$

First minimize the expression. Then, use only 2-to-1 multiplexers for the implementation. The inputs a, b, and *c* are available only in their non-inverted form, as well as constants 0 and 1.

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P8 (15 points). Given $P(A,B,C,D) = BCD + A\bar{B}C + \overline{(A+C+D)(B+D)}$

a. Implement this function using one 8-to-1 MUX and any number of NOT gates.

b. Implement this function using one 4-to-1 MUX with A and B as the select lines and a minimal number of AND/OR/NOT gates.

c. Implement this function using one 4-to-1 MUX with B and C as the select lines.