CprE 2810 HW08
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Latches and Flip-Flops

Due Date: Oct. 28, 2024

P1 (15 points) Draw the complete circuit diagram for each of these components using logic gates (no black boxes please):

a) SR Latch

b) Gated SR Latch

c) Gated D Latch

P2 (10 points) Draw the circuit diagram for a Negative-edge-triggered JK Flip-Flop. You are not allowed to use any high-level abstractions (e.g., latches) in this problem. You must use only logic gates.

P3 (10 points) Design a T Flip-Flop (**TFF**) using a D Flip-Flop (**DFF**). Draw the schematic diagram. The circuit designed must fully support all the functionalities provided by the TFF (PRESET and CLEAR implementations are not necessary and can be skipped), but the circuit must use only one DFF and one 2-to-1 MUX.

P4 (10 points) Design a D Flip-Flop (**DFF**) using a T Flip-Flop (**TFF**). Draw the schematic diagram. The circuit designed must fully support all the functionalities provided by the DFF (PRESET and CLEAR implementations are not necessary and can be skipped).

P5 (10 points) Describe the difference between the **Clk** signal in the gated D latch and the **Clock** signal in the D Flip-Flop. Under what conditions do they affect the behavior of the corresponding circuit?

P6 (10 points) Explain the meaning of the **Preset_n** and **Clear_n** signals to a D Flip-Flop. Describe how they affect the behavior of the circuit.

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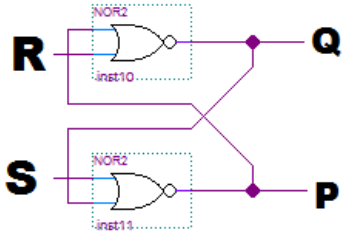
P7 (15 points) Use an SR latch and some additional logic gates to implement an LM-latch, which is defined with this characteristic table:

L	M	Q	P
0	0	0	1
0	1	No change	No change
1	0	No change	No change
1	1	1	0

a) (5 points) Complete the characteristic table for the SR Latch shown below



S	R	Q	P
0	0		
0	1		
1	0		
1	1		

b) (5 points) Write the values of **S** and **R** that produce the output combinations for each input combination to the LM-latch described by characteristic table shown above.

L	M	S	R	Q	P
0	0			0	1
0	1			No change	No change
1	0			No change	No change
1	1			1	0

c) (5 points) Use the table from part b) to derive Boolean expressions for **S** and **R** in terms of **L** and **M**. Then, draw the circuit for the LM-latch using logic gates.

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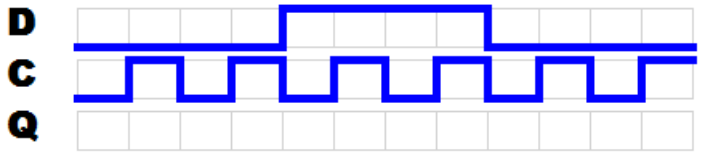
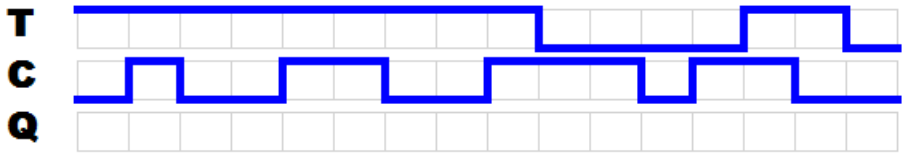
P8 (20 points) Complete the timing diagrams for the specified flip-flops. In all cases the Clock signal is labeled C. You may assume that Q is initially at 0 unless specified otherwise (as in part c).

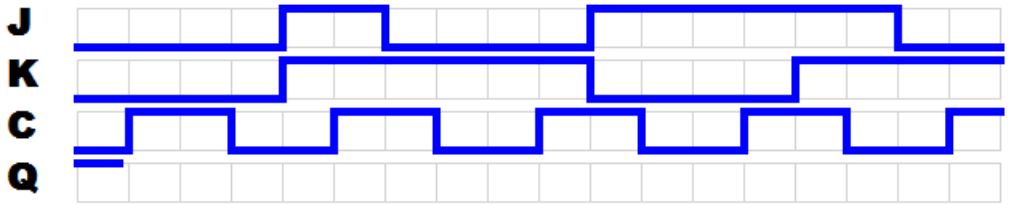
a) A positive-edge-triggered D Flip-Flop (DFF).



b) A negative-edge-triggered T Flip-Flop (TFF).



c) A positive-edge-triggered JK Flip-Flop (JKFF).



d) A negative-edge-triggered DFF with active-low Preset (P). Note that preset occurs when P=0.