CprE 2810 HW09
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Practice for Midterm 2

Due Date: Nov. 4, 2024

1. Binary Addition and Subtraction (4 x 3pt = 12 points):
Convert the following integers into binary numbers and perform the addition or subtraction in 2's complement representation. Write your answers and all intermediary steps to the right of each problem. Use 5-bit numbers for all problems and indicate if any bits need to be ignored.

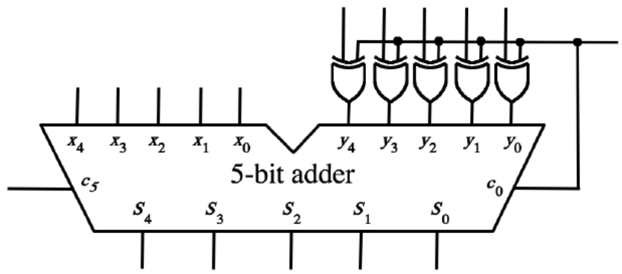
a)
```
   (+3)
+
   (+8)
------
```

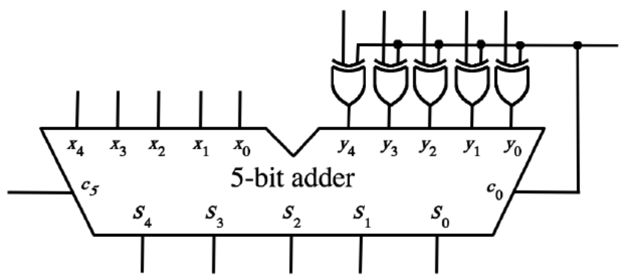
b)
```
   (-3)
+
   (-7)
------
```

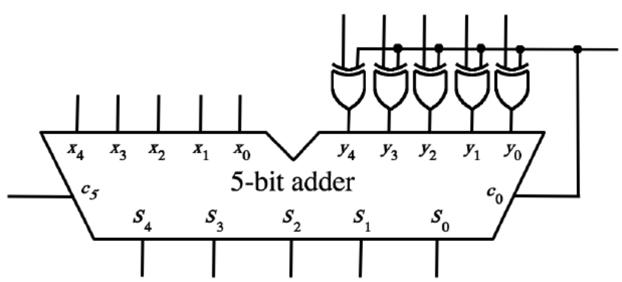
c)
```
   (+2)
-
   (+6)
------
```

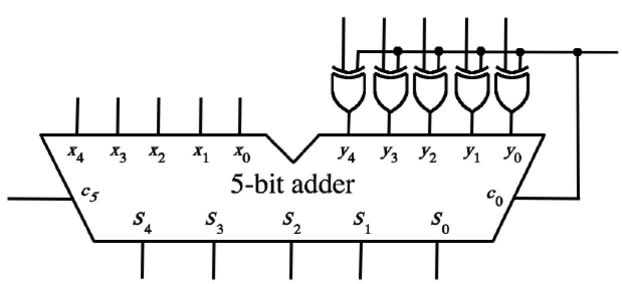
d)
```
   (-1)
-
   (-7)
------
```

2. Adders (4 x 2pt = 8 points). For each sub-problem in question 1, show the values of all input and output pins in the 5-bit adder/subtractor circuit.









3. Number Conversions (4 x 5 = 20 points)
(a) Convert 124_{10} to hexadecimal.

(b) Convert the following 32-bit float number (in IEEE 754 format) to decimal.
1 1 0 0 0 0 0 1 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

(c) Write down the 32-bit floating point representation (in IEEE 754 format) for 11.5

(d) Convert -55_{10} to an 8-bit binary number in 2's complement representation.

4. Multiplexers and decoder (15 points)
a) Draw the truth table for this function: $f(x, y, z) = xy\bar{z} + (\overline{x + y})z$

b) Implement this function using **only** 2-to-1 multiplexers and no other logic gates. Assume that the signals x, y, and z are available **only** in their non-inverted form. You can also assume that you have access to the constants 0 and 1. Clearly label all inputs, outputs, and pins.

c) Implement this function using a 4-to-1 multiplexer and one XOR gate. Clearly label all inputs, outputs, and pins of the decoder.

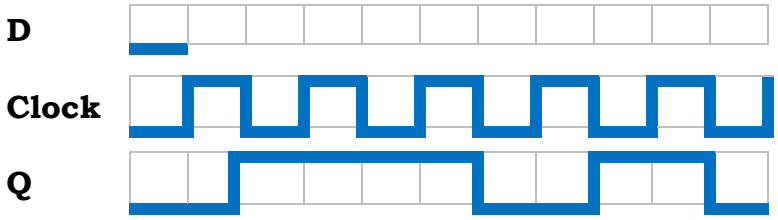
5. Full Adder (15 points)

a) Draw the truth table for a full adder with inputs x_i, y_i, and c_i and outputs c_{i+1} and s_i. (5p)

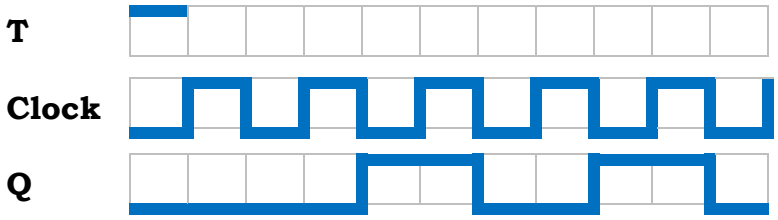
b) Implement a full adder with a minimal number of 2-to-1 multiplexers and no other logic gates. Assume that the input signals are available only in their non-inverted form, along with the constants 0 and 1. Clearly label all inputs, outputs, and pins of your circuit. (10p)

6. Flip-Flops and Timing Diagrams (15 points)
Complete the timing diagram for the specified flip-flop such that the output Q will be as indicated. Assume that the input signal can change only on the vertical lines. Also, assume that the setup time t_{su} and the hold time t_h are each equal to the width of one square.

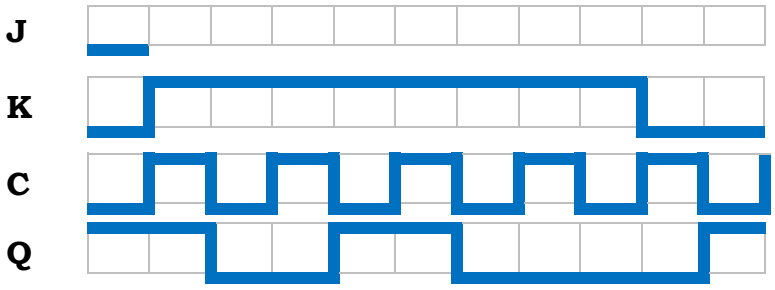
a) Complete the timing diagram for the D input to a negative-edge triggered D flip-flop.



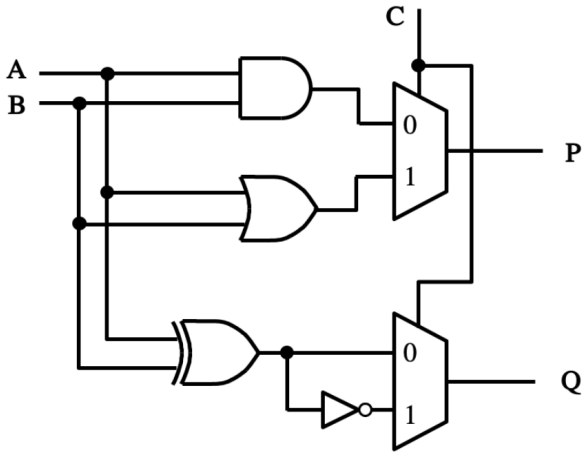
b) Complete the timing diagram for the T input to a negative-edge triggered T flip-flop.



c) Complete the timing diagram for the J input to a negative-edge triggered JK flip-flop.



7. Equivalent circuits (15 points).



a) Draw the truth table for the outputs P and Q as functions of A, B, and C.

b) Use K-maps to find the minimum-cost SOP expressions for P and Q.

c) What type of familiar circuit is this equivalent to? Explain.