CprE 2810 HW12
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Counters, Analysis of Syn. Seq. Circuits, ASM charts/examples
Finish by Dec 2, 2024

Instructions

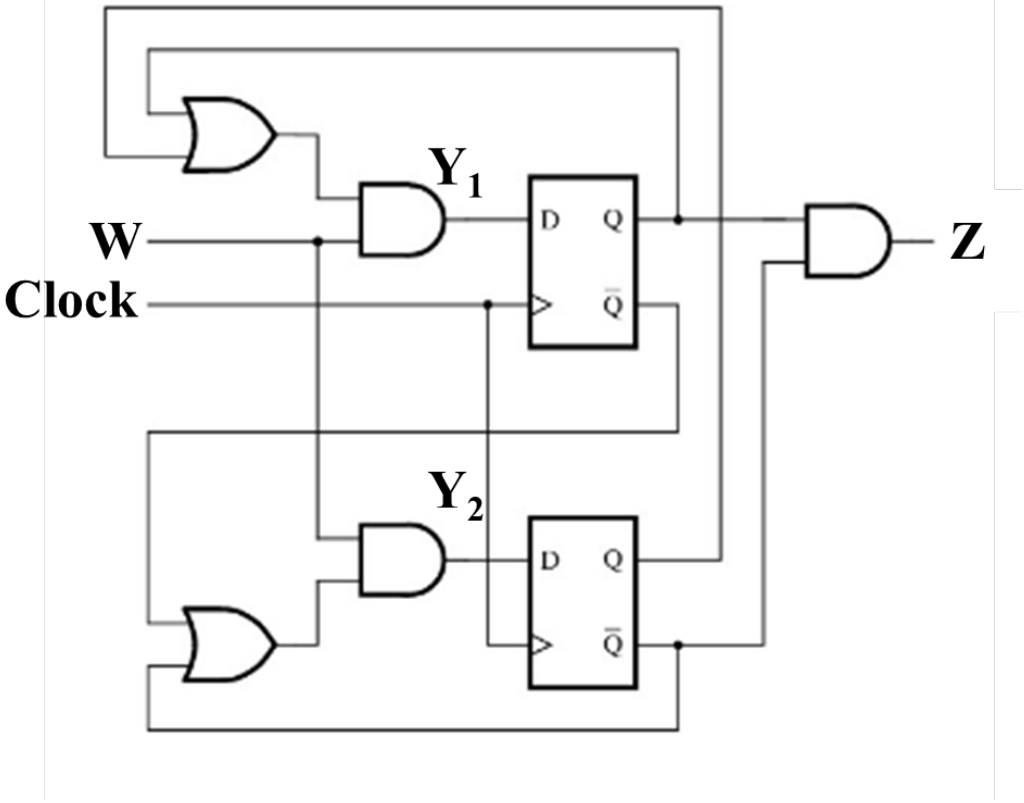
Complete the questions below to the best of your ability. Upload a PDF of your work to canvas.

Questions

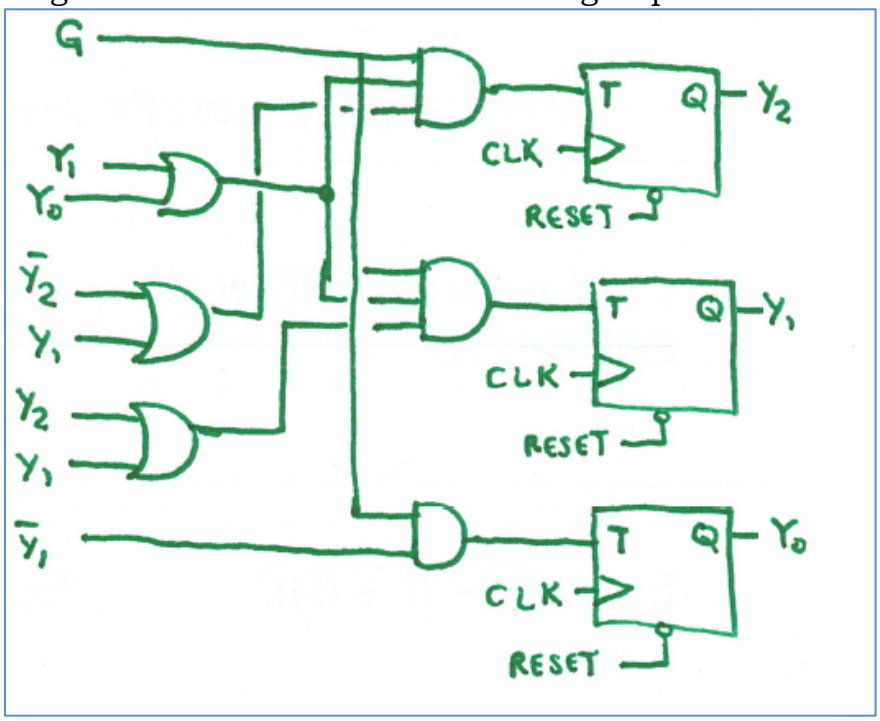
P1 (20 points): Design a 2-bit synchronous up-counter. Draw the state diagram/graph, the state table, and the state-assigned table. Then, use K-maps to derive logic expressions for the input and output logic. Finally, draw the circuit diagram using D Flip-Flops and any other logic gates. Label all inputs, outputs, and pins.

P2 (10 points): Consider a state machine that detects if a number (F) is a multiple of three (3, 6, 9, etc.). Draw the specified ASM chart that will output Z=1 based on the input W. Let F be the number of clock cycles for which the input W has been one. Draw a Moore type ASM chart that outputs Z=1 if F is a multiple of 3.

P3 (25 points): Derive the state table for the following circuit. What sequence of input values on wire W is detected by this circuit?



P4 (20 points): The FSM below looks like a counter. Draw a state diagram which illustrates its counting sequence.



P5 (25 points): Design a FSM with no inputs (other than CLK and RESETN) and four-bit output Z such that the FSM outputs the sequence 2, 3, 4, 5, 9, 13. The state assignments should be equal to the output and your circuit should use four positive-edge-triggered JKFFs and a minimal number of other gates.

A. Draw a state diagram. Don't forget the reset signal.

B. Draw the state-assigned table. This table should also include the excitation for the JKFFs (the values for J and K along with the next state values).

C. Draw K-maps to show that the inputs to the JKFF are as follows:
$J_3 = s_2 s_0, K_3 = s_2, J_2 = s_0, K_2 = s_0, J_1 = s_3 s_2, K_1 = s_0, J_0 = 1, K_0 = s_3 s_2 + s_1$

D. How might JKFF 2 be simplified given that both of its inputs are the same?