

Name and Student ID: \_\_\_\_\_ Lab Section: \_\_\_\_\_

Date: \_\_\_\_\_

### PRELAB:

**Q1.** Fill in the Truth Table below for an AND gate:

A	B	C
0	0	
0	1	
1	0	
1	1	

**Q2.** What does the .bdf file extension stand for?

**Q3.** What is the name of the FPGA on the DE2-115 board?

TA Initials: \_\_\_\_\_

### LAB:

**2.0** Fill in the Truth Table for *lab1step1*:

A	B	C
0	0	
0	1	
1	0	
1	1	

Logic Expression: \_\_\_\_\_

Quartus Simulation TA Initials: \_\_\_\_\_ Questa ModelSim TA Initials: \_\_\_\_\_

**4.0 Fill in the Truth Table for *lab1step2*:**

W	X	Y	Z
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Logic Expression: \_\_\_\_\_

TA Initials: \_\_\_\_\_

**4.0 Fill in the Truth Table for *lab1step3*:**

A	B	C	F

Logic Expression: \_\_\_\_\_

TA Initials: \_\_\_\_\_