General Description

The Virtex™-5 family provides the newest most powerful features in the FPGA market. Using the second generation ASMBL™ (Advanced Silicon Modular Block) column-based architecture, the Virtex-5 family contains four distinct platforms (sub-families), the most choice offered by any FPGA family. Each platform contains a different ratio of features to address the needs of a wide variety of advanced logic designs. Virtex-5 LX platform is the first to be introduced. This overview contains detailed information about the LX platform only. In addition to the most advanced, high-performance logic fabric, Virtex-5 LX platform contain many hard-IP system-level blocks, including powerful 36-Kbit block RAM/FIFOs, second generation 25 x 18 DSP slices, SelectIO™ technology with built-in digitally-controlled impedance, ChipSync™ source-synchronous interface blocks, enhanced clock management tiles with integrated Digital Clock Managers (DCM) and phase-locked-loop (PLL) clock generators, and advanced configuration options. Future platforms will contain high-performance PowerPC™ microprocessor cores, tri-mode Ethernet MACs (Media Access Controllers), and advanced serial connectivity. These features allow advanced logic designers to build the highest levels of performance and functionality into their FPGA-based systems. Built on a 65-nm state-of-the-art copper process technology, Virtex-5 FPGAs are a programmable alternative to custom ASIC technology. Most advanced system designs require the programmable strength of FPGAs. Virtex-5 FPGAs offer the best solution for addressing the needs of high-performance logic designers, high-performance DSP designers, and high-performance embedded systems designers with unprecedented logic, DSP, hard/soft microprocessor, and connectivity capabilities.

Summary of Virtex-5 Features

- Four platforms
  - Virtex-5 LX: High-performance general logic applications
  - Future platforms will be optimized for advanced serial connectivity, signal processing applications, and embedded systems
- Most advanced, high-performance, optimal utilization, FPGA fabric
  - True 6-input look-up table (LUT) technology
  - Dual 5-LUT option
  - Improved reduced-hop routing
  - 64-bit distributed RAM option
  - SRL32/Dual SRL16 option
- Powerful clock management tile (CMT) clocking
  - Digital Clock Manager (DCM) blocks for zero delay buffering, frequency synthesis, and clock phase shifting
  - PLL blocks for input jitter filtering, zero delay buffering, frequency synthesis, and phase-matched clock division
- Advanced DSP48E slices
  - 25 x 18, two's complement, signed multiplication
  - Optional adder/accumulator
  - Optional pipelining
  - Optional bitwise logical functionality
  - Dedicated cascade connections

- 36-Kbit block RAM/FIFOs
  - True dual-port RAM blocks
  - Enhanced optional programmable FIFO logic
  - Programmable
    - True dual-port widths up to x36
    - Simple dual-port widths up to x72
  - Built-in optional error-correction circuitry with scrubbing
  - Optionally program each block as two independent 18-Kbit blocks
- High-performance parallel SelectIO technology
  - 1.2 to 3.3V I/O Operation
  - Source-synchronous interfacing using ChipSync technology
  - Digitally-controlled impedance (DCI) active termination
  - Flexible fine-grained I/O banking
  - High-speed memory interface support
- Flexible configuration options
  - SPI-4 Parallel FLASH interface
  - Multi-bitstream support with dedicated fallback reconfiguration logic
  - Auto buswidth detection capability
- 65-nm copper CMOS process technology
- 1.0V core voltage
- High signal-integrity flip-chip packaging available in standard or Pb-free package options

Table 1: **Virtex-5 LX FPGA Family Members**

Device	Configurable Logic Blocks (CLBs)			DSP48E Slices[2]	Block RAM Blocks			CMTs[4]	Total I/O Banks	Max User I/O
	Array (Row x Col)	Virtex-5 Slices[1]	Max Distributed RAM (Kb)		18 Kb[3]	36 Kb	Max (Kb)			
XC5VLX30	80 x 30	4,800	320	32	64	32	1,152	2	13	400
XC5VLX50	120 x 30	7,200	480	48	96	48	1,728	6	17	560
XC5VLX85	120 x 54	12,960	840	48	192	96	3,456	6	17	560
XC5VLX110	160 x 54	17,280	1,120	64	256	128	4,608	6	23	800
XC5VLX220	160 x 108	34,560	2,280	128	384	192	6,912	6	23	800
XC5VLX330	240 x 108	51,840	3,420	192	576	288	10,368	6	35	1,200

Notes:
1. Virtex-5 slices are organized differently from previous generations. Each Virtex-5 slice contains four LUTs and four flip-flops (previously it was two LUTs and two flip-flops.)
2. Each DSP48E slice contains a 25 x 18 multiplier, an adder, and an accumulator.
3. Virtex-5 block RAMs are fundamentally 36 Kbits in size. Each block can also be used as two independent 18-Kbit blocks.
4. Each Clock Management Tile (CMT) contains two DCMs and one PLL.

Virtex-5 Logic Fabric

- Up to 50% speed improvement
- On average, one to two speed grade improvement over Virtex-4 devices
- Cascadable 32-bit variable shift registers or 64-bit distributed memory capability
- Superior routing architecture with enhanced diagonal routing supports block-to-block connectivity with minimal hops
- Up to 330,000 logic cells including:
  - Up to 207,360 internal fabric flip-flops with clock enable (XC5VLX330)
  - Up to 207,360 true 6-input look-up tables (LUTs) with greater than 13 million total LUT bits
  - Two outputs for dual 5-LUT mode gives enhanced utilization
  - Logic expanding multiplexers and I/O registers

550 MHz Clock Technology

- Up to six Clock Management Tiles (CMTs)
  - Each CMT contains two DCMs and one PLL/PMCD — up to eighteen total clock generators
  - Flexible DCM-to-PLL or PLL-to-DCM cascade
  - Precision clock deskew and phase shift
  - Flexible frequency synthesis
  - Multiple operating modes to ease performance trade-off decisions
  - Improved maximum input/output frequency
  - Fine-grained phase shifting resolution
  - Input jitter filtering
  - Low-power operation
  - Wide phase shift range
  - Phase-Matched Clock Divider (PMCD) functionality
- Differential clock tree structure for optimized low-jitter clocking and precise duty cycle
- 32 global clock networks
- Regional, I/O, and local clocks in addition to global clocks

550 MHz Integrated Block Memory

- Up to 10.3 Mbits of integrated block memory in the LX platform
- 36-Kbit blocks with optional dual 18-Kbit mode
- True dual-port RAM cells
- Independent port width selection (x1 to x72)
    - Up to x36 total per port for true dual port operation
    - Up to x72 total per port for simple dual port operation (one Read port and one Write port)
    - Memory bits plus parity/sideband memory support for x9, x18, x36, and x72 widths
    - Configurations from 32K x 1 to 512 x 72 (8K x 4 to 512 x 72 for FIFO operation)
- Multirate FIFO support logic
    - Full and Empty flag with fully programmable Almost Full and Almost Empty flags
- Synchronous FIFO support without Flag uncertainty
- Optional pipeline stages for higher performance
- Byte-write capability
- Dedicated cascade routing to form 64K x 1 memory without using FPGA routing
- Integrated optional ECC for high-reliability memory requirements
    - Optional ECC scrubbing support
- Special reduced-power design for 18 Kbit and below operation

550 MHz DSP48E Slices

- Dedicated 25-bit x 18-bit multiplier
- Optional pipeline stages for enhanced performance
- Optional 48-bit accumulator for multiply accumulate (MACC) operation with optional accumulator cascade to 96-bits
- Integrated adder for complex-multiply or multiply-add operation
- Optional bitwise logical operation modes
- Independent C registers per slice
- Fully cascadable in a DSP column without external routing resources

SelectIO Technology

- Up to 1,200 user I/Os
- Wide selection of I/O standards from 1.2V to 3.3V
- Extremely high-performance
    - Up to 800 Mb/s HSTL and SSTL (on all single-ended I/Os)
    - Up to 1.25 Gb/s LVDS (on all differential I/O pairs)
- True differential termination on-chip
- Same edge capture at input and output I/Os
- Extensive memory interface support

ChipSync Source-Synchronous Interfacing Logic

- Works in conjunction with SelectIO technology to simplify source-synchronous interfaces
- Per-bit deskew capability built into all I/O blocks (variable delay line on all inputs and outputs)
- Dedicated I/O and regional clocking resources (pins and trees)
- Built-in data serializer/deserializer logic with corresponding clock divider support in all I/O
- Networking/telecommunication interfaces up to 1.25 Gb/s

Digitally Controlled Impedance (DCI) Active I/O Termination

- Optional series or parallel termination
- Temperature and voltage compensation
- Makes board layout much easier
    - Reduces resistors
    - Places termination in the ideal location, at the signal source or destination

Configuration

- Support for Platform Flash, standard SPI Flash, or standard parallel NOR Flash configuration
- Bitstream support with dedicated fallback reconfiguration logic
- 256-bit AES bitstream decryption provides intellectual property security and prevents design copying
- Improved bitstream error detection/correction capability
- Auto Buswidth detection capability
- Partial Reconfiguration via ICAP port

65-nm Copper CMOS Process

- 1.0V Core Voltage
- 12-layer metal provides maximum routing capability and accommodates hard-IP immersion
- Triple-oxide technology for proven reduced static power consumption

Advanced Flip-Chip Packaging

- Pre-engineered packaging technology for proven superior signal integrity
    - Minimized inductive loops from signal to return
    - Optimal signal-to-PWR/GND ratios
- Reduces SSO induced noise by up to 7x
- Pb-Free and standard packages

Architectural Description

Virtex-5 Array Overview

Virtex-5 devices are user-programmable gate arrays with various configurable elements and embedded cores optimized for high-density and high-performance system designs. Virtex-5 devices implement the following functionality:

- I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by programmable I/O blocks (IOBs). The IOBs can be connected to very flexible ChipSync logic for enhanced source-synchronous interfacing. Source-synchronous optimizations include per-bit deskew (on both input and output signals), data serializers/deserializers, clock dividers, and dedicated I/O and local clocking resources.

- Configurable Logic Blocks (CLBs), the basic logic elements for Xilinx FPGAs, provide combinatorial and synchronous logic as well as distributed memory and SRL32 shift register capability. Virtex-5 CLBs are based on true 6-input look-up table technology and provide superior capabilities and performance compared to previous generations of programmable logic.

- Block RAM modules provide flexible 36 Kbit true dual-port RAM that are cascadable to form larger memory blocks. In addition, Virtex-5 block RAMs contain optional programmable FIFO logic for increased device utilization. Each Virtex-5 block RAM can also be configured as two independent 18 Kbit true dual-port RAM blocks, providing memory granularity for designs needing smaller RAM blocks.

- Cascadable embedded DSP48E slices with 25-bit x 18-bit dedicated multipliers, integrated adder, and 48-bit accumulator provide massively parallel DSP algorithm support. In addition, each DSP48E slice can be used to perform bitwise logical functions.

- Clock Management Tile (CMT) blocks provide the most flexible, highest-performance clocking for FPGAs. Each CMT contains two Digital Clock Manager (DCM) blocks (self-calibrating, fully digital), and one PLL/PMCD block (self-calibrating, analog) for clock distribution delay compensation, clock multiplication/division, coarse-/fine-grained clock phase shifting, and input clock jitter filtering.

Virtex-5 Features

This section briefly describes the features of the Virtex-5 family of FPGAs.

Input/Output Blocks (SelectIO)

IOBs are programmable and can be categorized as follows:

- Programmable single-ended or differential (LVDS) operation
- Input block with an optional single data rate (SDR) or double data rate (DDR) register
- Output block with an optional SDR or DDR register
- Bidirectional block
- Per-bit deskew circuitry
- Dedicated I/O and regional clocking resources
- Built in data serializer/deserializer

The IOB registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended standards:

- LVTTL
- LVCMOS (3.3V, 2.5V, 1.8V, 1.5V, and 1.2V)
- PCI (33 and 66 MHz)
- PCI-X
- GTL and GTLP
- HSTL 1.5V and 1.8V (Class I, II, III, and IV)
- HSTL 1.2V (Class 1)
- SSTL 1.8V and 2.5V (Class I and II)

The Digitally Controlled Impedance (DCI) I/O feature can be configured to provide on-chip termination for each single-ended I/O standard and some differential I/O standards.

The IOB elements also support the following differential signaling I/O standards:

- LVDS and Extended LVDS (2.5V only)
- BLVDS (Bus LVDS)
- ULVDS
- Hypertransport™
- Differential HSTL 1.5V and 1.8V (Class I and II)
- Differential SSTL 1.5V and 1.8V (Class I and II)
- RSDS (2.5V point-to-point)

Two adjacent pads are used for each differential pair. Two or four IOB blocks connect to one switch matrix to access the routing resources.

Per-bit deskew circuitry allows for programmable signal delay internal to the FPGA. Per-bit deskew flexibly provides fine-grained increments of delay to carefully produce a range of signal delays. This is especially useful for synchronizing signal edges in source-synchronous interfaces.

General purpose I/O in select locations (eight per bank) are designed to be "regional clock capable" I/O by adding special hardware connections for I/O in the same locality. These regional clock inputs are distributed within a limited region to minimize clock skew between IOBs. Regional I/O clocking supplements the global clocking resources.

Data serializer/deserializer capability is added to every I/O to support source-synchronous interfaces. A serial-to-parallel converter with associated clock divider is included in the input path, and a parallel-to-serial converter in the output path.

An in-depth guide to the Virtex-5 IOB is found in the *Virtex-5 User Guide*.

Configurable Logic Blocks (CLBs)

A Virtex-5 CLB resource is made up of two slices. Each slice is equivalent and contains:

- Four function generators
- Four storage elements
- Arithmetic logic gates
- Large multiplexers
- Fast carry look-ahead chain

The function generators are configurable as 6-input LUTs or dual-output 5-input LUTs. SLICEMs in some CLBs can be configured to operate as 32-bit shift registers (or 16-bit x 2 shift registers) or as 64-bit distributed RAM. In addition, the four storage elements can be configured as either edge-triggered, D-type flip-flops or level sensitive latches. Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

The Virtex-5 CLBs are further discussed in the *Virtex-5 User Guide*.

Block RAM

The 36 Kbit true dual-port RAM block resources are programmable from 32K x 1 to 512 x 72, in various depth and width configurations. In addition, each 36-Kbit block can also be configured to operate as two, independent 18-Kbit dual-port RAM blocks.

Each port is totally synchronous and independent, offering three "read-during-write" modes. Block RAM is cascadable to implement large embedded storage blocks. Additionally, back-end pipeline registers, clock control circuitry, built-in FIFO support, ECC, and byte write enable features are also provided as options.

The block RAM feature in Virtex-5 devices is further discussed in the *Virtex-5 User Guide*.

DSP48E Slices

DSP48E slice resources contain a dedicated 25 x 18-bit two's complement signed multiplier, adder logic, and a 48-bit accumulator. Each multiplier or accumulator can be used independently. Each DSP48E slice also contains extensive cascade capability to efficiently implement high-speed DSP algorithms.

The Virtex-5 DSP48E slice features are further discussed in *Virtex-5 XtremeDSP Design Considerations*.

Global Clocking

The CMTs and global-clock multiplexer buffers provide a complete solution for designing high-speed clock networks.

Each CMT contains two DCMs and one PLL/PMCD. The DCMs and PLL/PMCDs can be used independently or extensively cascaded. Up to six CMT blocks are available, providing up to eighteen total clock generator elements.

Each DCM provides familiar clock generation capability. To generate deskewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90°, 180°, and 270° phase-shifted versions of the output clocks. Fine-grained phase shifting offers higher-resolution phase adjustment with fraction of the clock period increments. Flexible frequency synthesis provides a clock output frequency equal to a fractional or integer multiple of the input clock frequency.

To augment the DCM capability, Virtex-5 CMTs also contain a PLL/PMCD. This block provides reference clock jitter filtering and further frequency synthesis options.

Virtex-5 devices have 32 global-clock MUX buffers. The clock tree is designed to be differential. Differential clocking helps reduce jitter and duty cycle distortion.

Routing Resources

All components in Virtex-5 devices use the same interconnect scheme and the same access to the global routing matrix. In addition, the CLB-to-CLB routing is designed to offer a complete set of connectivity in as few hops as possible. Timing models are shared, greatly improving the predictability of the performance for high-speed designs.

Boundary Scan

Boundary Scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-5 devices, complying with IEEE standards 1149.1 and 1532.

Configuration

Virtex-5 devices are configured by loading the bitstream into internal configuration memory using one of the following modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary Scan mode (IEEE-1532 and -1149)
- SPI mode (Serial Peripheral Interface standard Flash)
- BPI-up/BPI-down modes (Byte-wide Peripheral interface standard x8 or x16 NOR Flash)

In addition, Virtex-5 devices also support the following configuration options:

- 256-bit AES bitstream decryption for IP protection
- Multi-bitstream management (MBM) for cold/warm boot support
- Parallel configuration bus width auto-detection
- Parallel daisy chain
- Configuration CRC and ECC support for the most robust, flexible device integrity checking

Virtex-5 device configuration is further discussed in the *Virtex-5 Configuration Guide*.

Intellectual Property Cores

Xilinx offers IP cores for commonly used complex functions including DSP, bus interfaces, processors, and processor peripherals. Using Xilinx LogiCORE™ products and cores from third party AllianceCORE participants, customers can shorten development time, reduce design risk, and obtain superior performance for their designs. Additionally, our CORE Generator™ system allows customers to implement IP cores into Virtex-5 FPGAs with predictable and repeatable performance. It offers a simple user interface to generate parameter-based cores optimized for our FPGAs.

The System Generator for DSP tool allows system architects to quickly model and implement DSP functions using handcrafted IP and features an interface to third-party system level DSP design tools. System Generator for DSP implements many of the high-performance DSP cores supporting Virtex-5 FPGAs including the Xilinx Forward Error Correction Solution with Interleaver/De-interleaver, Reed-Solomon encoder/decoders, and Viterbi decoders. These are ideal for creating highly-flexible, concatenated codecs to support the communications market.

Industry leading connectivity and networking IP cores include leading-edge PCI Express, Serial RapidIO, Fibre Channel, and 10Gb Ethernet cores using Virtex-5 RocketIO serial transceivers. The Xilinx SPI-4.2 IP core utilizes the Virtex-5 ChipSync technology to implement dynamic phase alignment for high-performance source-synchronous operation. Xilinx also provides PCI cores for advanced system-synchronous operation.

MicroBlaze™ 32-bit core provides the industry's fastest soft processing solution for building complex systems for the networking, telecommunication, data communication, embedded, and consumer markets. The MicroBlaze processor features a RISC architecture with Harvard-style separate 32-bit instruction and data buses running at full speed to execute programs and access data from both on-chip and external memory. A standard set of peripherals are also CoreConnect™ enabled to offer MicroBlaze designers compatibility and reuse.

All IP cores for Virtex-5 FPGAs are found on the Xilinx IP Center Internet portal presenting the latest intellectual property cores and reference designs using Smart Search for faster access.

Application Notes and Reference Designs

Application notes and reference designs written specifically for the Virtex-5 family are available on the Xilinx website after product introduction at:

http://www.xilinx.com/virtex5

Virtex-5 Device and Package Combinations and Maximum I/Os

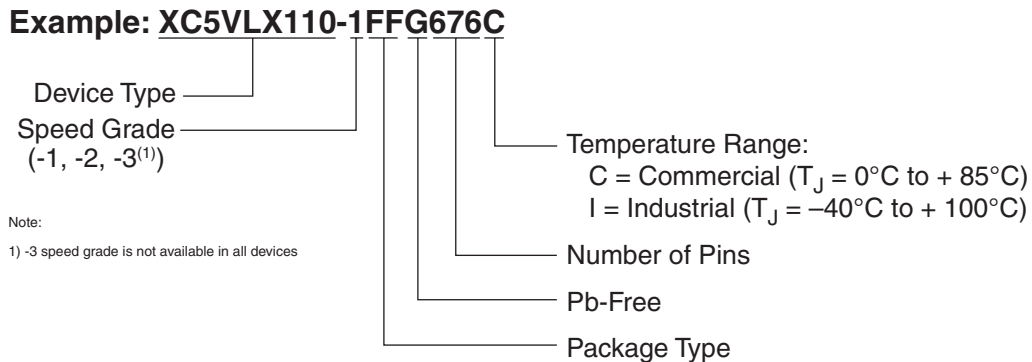*Table 2:* **Virtex-5 Device and Package Combinations and Maximum Available I/Os**

Package	FF324 FFG324	FF676 FFG676	FF1153 FFG1153	FF1760 FFG1760
Size (mm)	19 x 19	27 x 27	35 x 35	42.5 x 42.5
Device	I/O	I/O	I/O	I/O
XC5VLX30	220	400		
XC5VLX50	220	440	560	
XC5VLX85		440	560	
XC5VLX110		440	800	800
XC5VLX220				800
XC5VLX330				1,200

Notes:
1. Flip-chip packages are also available in Pb-Free versions (FFG).

Virtex-5 Ordering Information

Virtex-5 ordering information shown in Figure 1 applies to all packages including Pb-Free.

Example: XC5VLX110-1FFG676C

Device Type

Speed Grade
(-1, -2, -3[1])

Note:
1) -3 speed grade is not available in all devices

Temperature Range:
C = Commercial ($T_J = 0°C$ to + 85°C)
I = Industrial ($T_J = -40°C$ to + 100°C)

Number of Pins

Pb-Free

Package Type

DS100_01_031006

Figure 1: **Virtex-5 Ordering Information**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/14/06	1.0	Initial Xilinx release.
05/12/06	1.1	First version posted to the Xilinx website. Minor typographical edits and description updates to highlight new features. Removed LUT utilization bullet from **Virtex-5 Logic Fabric**, page 2.

Virtex-5 Documentation

Complete and up-to-date documentation of the Virtex-5 LX family of FPGAs is available on the Xilinx website. In addition to the most recent Virtex-5 Family Overview, the following files are also available for download:

Virtex-5 Data Sheet: DC and Switching Characteristics

This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5 family.

Virtex-5 User Guide

This guide includes chapters on:

- Clocking Resources
- Clock Management Technology (CMT)
- Phase-Locked Loops (PLL)
- Block RAM and FIFO memory
- Configurable Logic Blocks (CLBs)
- SelectIO Resources
- I/O Logic Resources
- Advanced I/O Logic Resources

Virtex-5 XtremeDSP Design Considerations

This guide describes the DSP48E slice and includes reference designs for using DSP48E math functions and various filters.

Virtex-5 Configuration Guide

This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.

Virtex-5 Packaging and Pinout Specifications

This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.