



CprE / ComS 583 Reconfigurable Computing

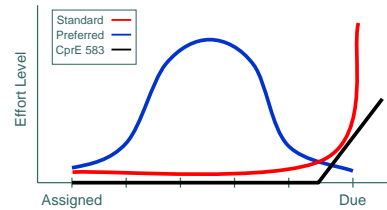
Prof. Joseph Zambreno
Department of Electrical and Computer Engineering
Iowa State University

Lecture #6 – Modern FPGA Devices



Quick Points

- HW #2 coming out over the weekend
 - Due Thursday, September 21 (12:00pm)
 - LUT mapping
 - Comparing FPGA devices
 - Synthesizing arithmetic operators

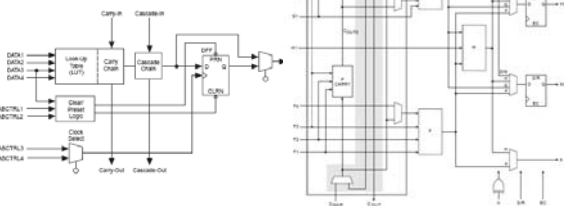


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Recap

- Hard-wired carry logic support



Altera FLEX 8000

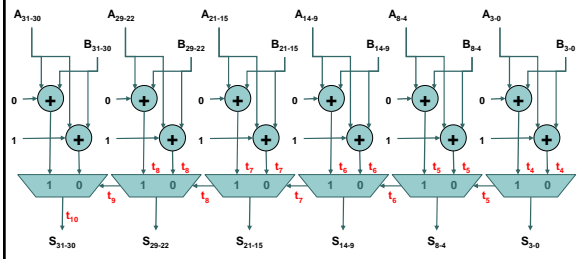
Xilinx XCV4000

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Recap (cont.)

- Square-root carry select adders

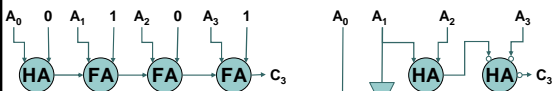


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Recap (cont.)

- If one operand is constant:
 - More speed?
 - Less hardware?

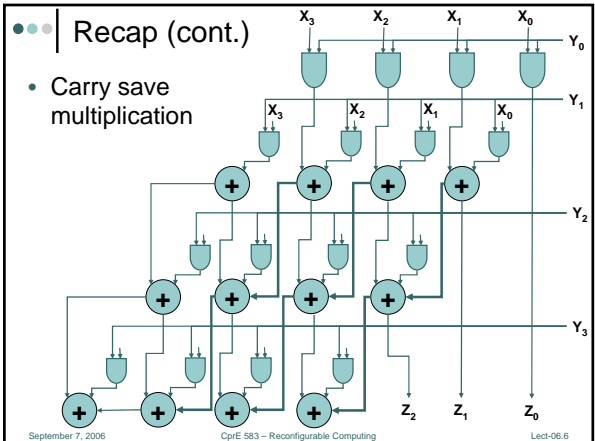


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Recap (cont.)

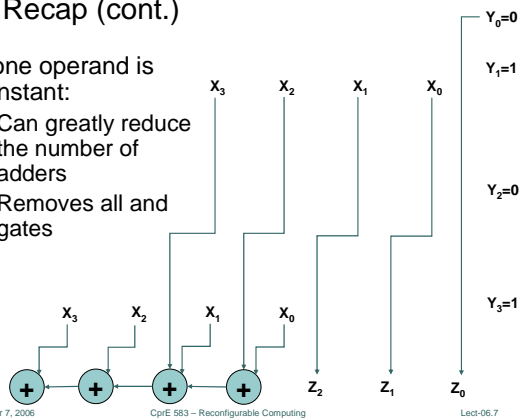
- Carry save multiplication



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Recap (cont.)

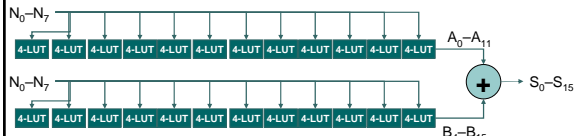
- If one operand is constant:
 - Can greatly reduce the number of adders
 - Removes all and gates



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LUT-Based Constant Multipliers

$$\begin{array}{r}
 10101011 \\
 \times \text{NNNNNNNN} \\
 \hline
 \text{AAAAAAAAAAAA} \quad (N * 1011 \text{ (LSN)}) \\
 + \text{BBBBBBBBBBBB} \quad (N * 1010 \text{ (MSN)}) \\
 \hline
 \text{SSSSSSSSSSSSSS} \quad \text{Product}
 \end{array}$$



- Constants can be changed in the LUTs to program new multipliers

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Outline

- Recap
- More Multiplication
- Handling Fractional Values
 - Fixed Point
 - Floating Point
- Some Modern FPGA Devices
 - Xilinx – XC5200, Virtex (-II / -II Pro / -4 / -5), Spartan (-II / -3)
 - *Altera – FLEX 10K, APEX (20K / II), ACEX 1K, Cyclone (II), Stratix (GX / II / II GX)

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Partial Product Generation

- AND gates in multiplication are wasteful
 - Option 1 – use cascade logic
 - Option 2 – break into smaller (2x2) multipliers

$$\begin{array}{r}
 42 = \quad \quad \quad 101010 \quad \text{Multiplicand} \\
 \times 11 = \quad \quad \times 1011 \quad \text{Multiplier} \\
 \hline
 \quad \quad \quad \quad \quad 0110 \quad (10 \times 11) \\
 \quad \quad \quad \quad \quad 0110 \quad (10 \times 11) \\
 \quad \quad \quad \quad \quad 0110 \quad (10 \times 11) \\
 \quad \quad \quad \quad \quad 0100 \quad (10 \times 10) \\
 \quad \quad \quad \quad \quad 0100 \quad (10 \times 10) \\
 \hline
 \quad \quad \quad + \quad 0100 \quad (10 \times 10) \\
 462 = \quad \quad \quad 0111001110 \quad \text{Product}
 \end{array}$$

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Representation Compression

- Multiplication can be simplified if the representation is compressed
 - Standard – binary representation $\{0,1\} \times 2^n$
 - Canonical Signed Digit (CSD) representation $\{-1,0,1\} \times 2^n$
- To encode CSD:
 - Set $C = (B + (B \ll 1))$
 - Calculate $-2C = 2^*(C \gg 1)$
 - $D_i = B_i + C_i - 2C_{i+1}$, where C_{i+1} is the carryout of $B_i + C_i$
- Example: $B = 61d = 0111101b$

$$\begin{array}{l}
 C = 0111101b + 01111010b = 010110111b \\
 -2C_{i+1} = 2222101 \\
 D = 1000201 = 1000(-1)01
 \end{array}$$
- For any n bit number, there can only be $n/2$ nonzero digits in a CSD representation (every other bit)

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Booth Encoding

- Variation on CSD encoding:

$$E_i = -2B_i + B_{i-1} + B_{i+2}$$
 - Select a group of 3 digits, add the two least significant digits, and then subtract $2x$ the most significant bit
 - E_i is $\{-2,-1,0,1\} \times 2^{2n}$
- Example:
 - $B = 61d = 0111101b = \underline{00}0111101\underline{0}b$ (with padding)
 - $E = 010(-1)1$
- Reduces the number of partial products for multiplication by $1/2$
- Can automatically handle negative numbers

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Fractional Arithmetic

- Many important computations require fractional components
- Fractional arithmetic often ignored in FPGA literature
 - Complex standards (ex. IEEE special cases)
 - Resource intensive and slow
- Why not just extend the binary representation past the decimal point?

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Fixed-Point Representation

- Separate value into Integer (I) and Fractional remainder (F)



- F bits represent $\{0,1\} \times 2^{-n}$
- How large to make I and F depends on application
 - Ex: Q16.16 is 16 bits of integer $[-2^{15}, 2^{16})$ with 16 bits of fraction – increments of 2^{-16} or 0.0000152587890625
 - Ex: Q1.127 is a normalized integer $[-1,1)$ with 127 bits of fraction – increments of 2^{-127} or 5.8774717541114375398436826861112e-39

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Fixed-Point Arithmetic

- Addition, subtraction the same (Q4.4 example):

```

3.6250    0011.1010
+ 2.8125  0010.1101
-----
6.4375    0110.0111
    
```

- Multiplication requires realignment:

```

3.6250          0011.1010
x 2.8125        0010.1101
-----
          00111010
          00111010
          00111010
          00111010
-----
10.1953125    1010.00110010
    
```

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Fixed-Point Issues

- Overflow/underflow
- Quantization Errors
 - After rounding down previous example
 - $3.625 \times 2.8125 = 10.1875$ (0.08% error)
 - In Q4.4, 2 divided by 3 = 0.625 (6.25% error)
- Scaling
- Dynamic range needed for some applications

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IEEE 754 Floating Point

- Single precision: $V = (-1)^S \times 2^{(E-127)} \times (1.F)$



- Double precision: $V = (-1)^S \times 2^{(E-1023)} \times (1.F)$



- Special conditions – not a number (NaN), +0, +infinity
- Gradual underflow

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Lect-06.17

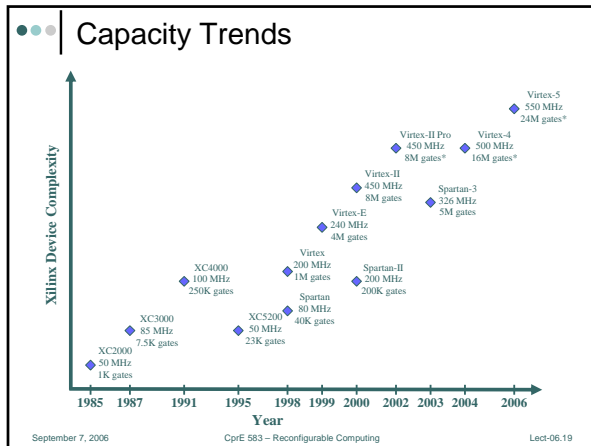
Floating Point FPGA Hardware

- Xilinx XCV4085
- Addition
 - Single-precision – 587 4-LUTs
 - Double-precision – 1334 4-LUTs
- Multiplication
 - Single-precision – 1661 4-LUTs
 - Double-precision – 4381 4-LUTs
- Division
 - Single-precision – 1583 4-LUTs
 - Double-precision – 4910 4-LUTs
- For double-precision, can only fit any two of three units on a single device!
- See [Und04] for details

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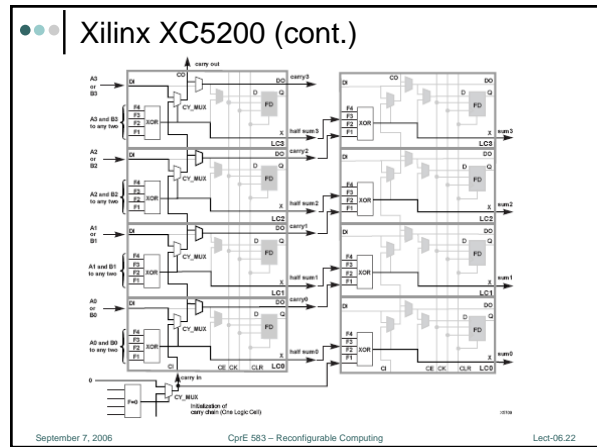
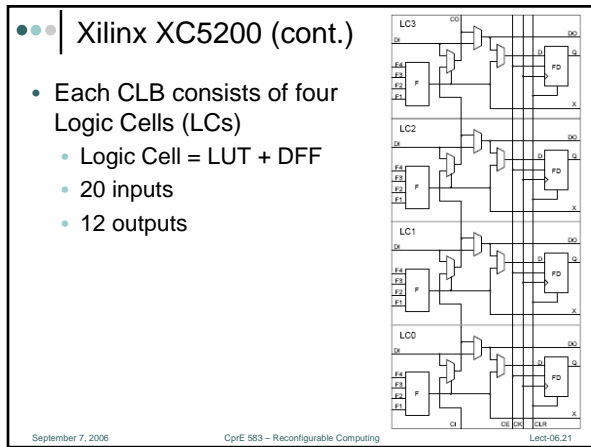


Xilinx XC5200 FPGA

- Successor to the XC4000
- Relatively small amount of CLBs with faster interconnect

Device	XC5202	XC5204	XC5206	XC5210	XC5215
Logic Cells	256	480	784	1,296	1,936
Max Logic Gates	3,000	6,000	10,000	16,000	23,000
VersaBlock Array	8 x 8	10 x 12	14 x 14	18 x 18	22 x 22
CLBs	64	120	196	324	484
Flip-Flops	256	480	784	1,296	1,936
I/Os	84	124	148	196	244

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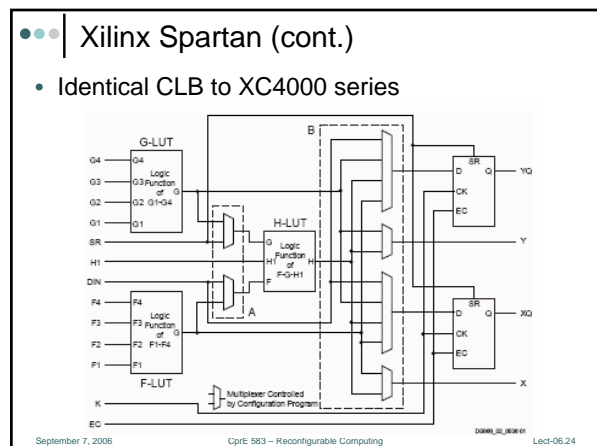


Xilinx Spartan FPGAs

- Meant to be low-power / low-cost version of XC4000 series (on newer process technology)

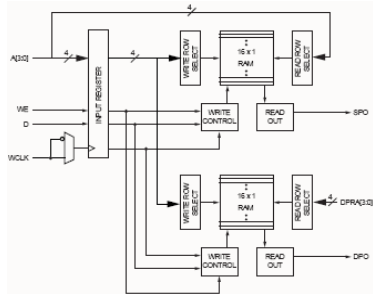
Device	XCS05	XCS10	XCS20	XCS30	XCS40
Logic Cells	238	466	950	1,368	1,862
Max Logic Gates	5,000	10,000	20,000	30,000	40,000
CLB Matrix	10 x 10	14 x 14	20 x 20	24 x 24	28 x 28
Total CLBs	100	196	400	576	784
Flip-Flops	360	616	1,120	1,536	2,016
I/Os	77	112	160	192	224
Dist. RAM Bits	3,200	6,272	12,800	18,432	25,088

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Xilinx Spartan (cont.)

- Individual LUTs can be programmed as 16x1 RAMs and combined to form larger memory structures



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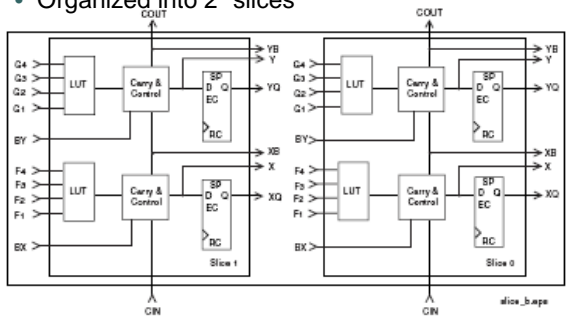
Xilinx Virtex FPGAs

Device	Logic Cells	Max Logic Gates	CLB Array	I/O Bits	Block RAM Bits	Select RAM+ Bits
XCV50	1,728	57,906	16 x 24	180	32,768	24,576
XCV100	2,700	108,904	20 x 30	180	40,960	38,400
XCV150	3,888	164,674	24 x 38	260	49,152	55,296
XCV200	5,292	238,666	28 x 42	284	57,844	75,264
XCV300	6,912	322,970	32 x 48	316	65,536	98,304
XCV400	10,800	468,252	40 x 60	404	81,920	153,600
XCV600	15,552	661,111	48 x 72	512	98,304	221,184
XCV800	21,168	888,439	56 x 84	512	114,688	301,058
XCV1000	27,648	1,124,022	64 x 96	512	131,072	393,216

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Xilinx Virtex (cont.)

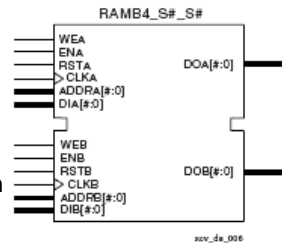
- 4 4-LUTs / FFs per CLB
- Organized into 2 “slices”



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Xilinx Virtex (cont.)

- Block Select+RAM – dedicated blocks of on-chip, true dual port read/write synchronous RAM
- 4Kbit of RAM with different aspect ratios
- Faster, less flexible than distributed RAM using LUTs



Virtex-E – updated, larger version of Virtex devices

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Xilinx Spartan-II

- CLB structure similar to Virtex

Device	Logic Cells	System Gates	CLB Array	I/O Bits	Distributed RAM Bits	Select RAM+ Bits
XC2S15	432	15,000	8 x 12	86	6,144	16,384
XC2S30	972	30,000	12 x 18	92	13,824	24,576
XC2S50	1,728	50,000	16 x 24	176	24,576	32,768
XC2S100	2,700	100,000	20 x 30	176	38,400	40,960
XC2S150	3,888	150,000	24 x 36	260	55,296	49,152
XC2S200	5,292	200,000	28 x 42	284	75,264	57,344

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Xilinx Virtex-II Platform FPGAs

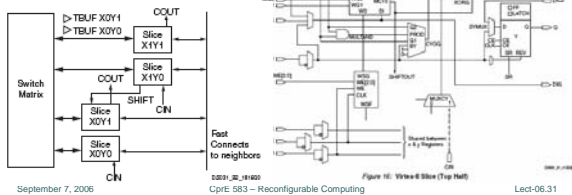
- “Platform” FPGA == Multiplier??

Device	Max Logic Gates	CLB Array	Multiplier Blocks	Max I/O Pads	Block RAM Bits	Select RAM+ Bits
XC2V40	40K	8 x 8	4	88	8K	72K
XC2V80	80K	16 x 8	8	120	16K	144K
XC2V250	250K	24 x 16	24	200	48K	432K
XC2V500	500K	32 x 24	32	264	96K	576K
XC2V1000	1M	40 x 32	40	432	160K	720K
XC2V1500	1.5M	48 x 40	48	528	240K	864K
XC2V2000	2M	56 x 48	56	624	336K	1,008K
XC2V3000	3M	64 x 56	96	720	448K	1,728K
XC2V4000	4M	80 x 72	120	912	720K	2,160K
XC2V6000	6M	96 x 88	140	1,104	1,056K	2,592K
XC2V8000	8M	112 x 104	168	1,108	1,456K	3,024K

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Xilinx Virtex-II (cont.)

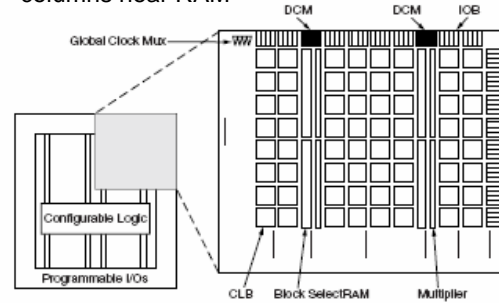
- 4 Slices per CLB, 2 4-LUTs per slice
- 8 LUTs per CLB
- Block Select+RAMs now 18Kbit each



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Xilinx Virtex-II (cont.)

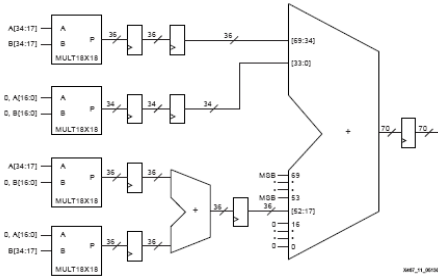
- Block multipliers (18b x 18b) arranged in columns near RAM



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Block Multipliers

- Synthesis tools can take larger multipliers and break them down into 18x18 multipliers



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Xilinx Virtex-II Pro FPGAs

Device	PowerPC CPU Blocks	Logic Cells	Multiplier Blocks	Max I/O Pads	Block RAM Bits	Select RAM+ Bits
XC2VP2	0	3,168	12	204	44K	216K
XC2VP4	1	6,768	28	348	94K	504K
XC2VP7	1	11,088	44	396	154K	792K
XC2VP20	2	20,880	88	564	290K	1,584K
XC2VP30	2	30,816	136	644	428K	2,448K
XC2VP40	2	43,632	192	804	606K	3,456K
XC2VP50	2	53,136	232	852	738K	4,176K
XC2VP70	2	74,448	328	996	1,034K	5,904K
XC2VP100	2	99,216	444	1,164	1,378K	7,992K

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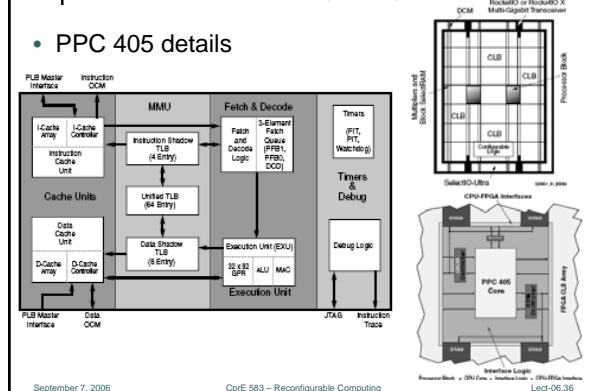
Xilinx Virtex-II Pro (cont.)

- PowerPC processor block features
 - 300+ MHz Harvard architecture (RISC)
 - Five-stage pipeline
 - Hardware multiply/divide
 - Thirty-two 32-bit GPRs
 - 16 KB two-way instruction cache
 - 16 KB two-way data cache
 - On-Chip Memory (OCM) interface
 - IBM CoreConnect (OPB, PLB) interfaces

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Xilinx Virtex-II Pro (cont.)

- PPC 405 details



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••• Xilinx Spartan-3 FPGAs

- CLB structure similar to Virtex-II

Device	System Gates	CLB Array	Multiplier Blocks	Max I/O Pads	Distr. RAM Bits	Select RAM+ Bits
XC3S50	50K	16 x 12	4	124	12K	72K
XC3S200	200K	24 x 20	12	173	30K	216K
XC3S400	400K	32 x 28	16	264	56K	288K
XC3S1000	1M	48 x 40	24	391	120K	432K
XC3S1500	1.5M	64 x 52	32	487	208K	576K
XC3S2000	2M	80 x 64	40	565	320K	720K
XC3S4000	4M	96 x 72	96	712	432K	1,728K
XC3S5000	5M	104 x 80	104	784	520K	1,872K

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Lect-06.37

••• Xilinx Virtex-4 FPGAs

- Comes in three varieties:
 - Virtex-4 **LX**: most amount of LUTs
 - Virtex-4 **FX**: has PowerPCs like V2P
 - Virtex-4 **SX**: contains most amount of XtremeDSP slices
- CLB structure similar to Virtex-II
 - Largest LX device – 89,088 slices = 178,176 4-LUTs!
 - FX devices limited to 2 PPC 405s like Virtex-II Pro
- XtremeDSP Slices:
 - Same 18x18 block multiplier, now with optional pipelining
 - Includes built-in 48-bit accumulator for MAC operations

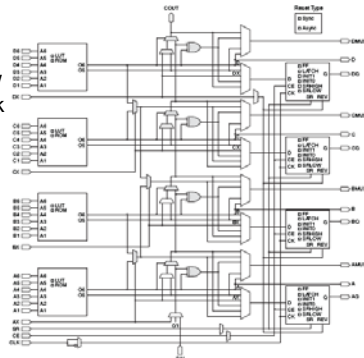
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Lect-06.38

••• Xilinx Virtex-5

- CLB slices uses 6-input LUTs
- Block RAMs now 36Kbits per block
- DSP slices now support 25x18 MAC
- Diagonal routing
- Only **LX** series available now



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Lect-06.39

••• Summary

- Handling fractional math in hardware is important, and expensive
 - Data point – 3 double-precision dividers in a Xilinx XC2VP30
 - Data point – cannot fit a double-precision multiplier in a Xilinx XC3S50
 - Fixed point an alternative, but not practical for all applications
- Xilinx FPGAs
 - 4-LUTs arranged in slices, CLBs (except for V5)
 - Physical SRAM blocks for fast memory
 - Physical multipliers for fast DSP operations
 - Some physical CPUs to manage embedded systems

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Lect-06.40